A Process-Dependent Worst-Case Analysis for MMIC Design Based on a Handy MESFET Simulator

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Abstract —**The design of inexpensive MMIC modules implies a practical use of worst-case analysis. A reliable method based on the unavoidable dispersion of uncorrelated technological parameters is proposed. The method relies on a convenient MESFET simulator which provides the dc, RF, and noise parameters for any bias conditions. The input data comprise geometrical or electrical information readily available to the designer. All the equations are given in detail. The results are compared with experimental data from several GaAs MMIC manufacturers. Finally the method is successfully applied to the design of a monolithic *C*-band amplifier. The forecasts of the worst-case analysis are compared with the experimental results. Measurements from different chips and from different wafers are presented and show a high RF yield.**

I. INTRODUCTION

AFTER A DECADE of an intensive research on their fabrication and characterization, monolithic microwave integrated circuits (MMIC's) are ready for increasing use in many systems in civil or military applications. With the emergence of the foundries, not only the experienced, but all the interested companies are able to plan the use of MMIC modules for coming programs.

Nowadays, the very first concern of most designers is the reduction of the cost per chip. A key factor is the tolerance of the design with respect to process uniformity. The aim is to minimize the number of fabrication runs to obtain a satisfactory circuit and then to maintain a high yield on the wafer, from wafer to wafer, and even from batch to batch. Hence arises the imperative need of a reliable worst-case analysis (WCA) of the circuit.

There are two different approaches for a conservative WCA. The first consists in measuring a large number of devices, extracting the elements of equivalent circuits, establishing correlation matrices between those elements, and finally using them statistically with powerful circuit analysis software [1]. Although this is certainly the most serious approach, it is very time consuming and it demands long experience with the circuit manufacturer. Unfortunately this is not always possible for a designer using a external commercial GaAs foundry.

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Sometimes the foundry provides the circuit designer with statistical dispersion of FET parameters but without correlation. Using those data leads to very pessimistic predictions of circuit performance, predictions that are almost meaningless, as will be shown in this paper.

The other approach is to perform the WCA from process-dependent parameters only [2], [3], such as the gate length, doping density, and layer thickness beneath the gate of the MESFET. The strong advantage of this method is that those parameters are uncorrelated.

Table I gives some examples of the dependence of MMIC element parameters on fabrication operations. From this table it is clearly seen that the MESFET is the more sensitive element in MMIC fabrication. Although dispersions on passive elements have to be considered in a complete WCA, only the aspects concerning the MESFET are investigated in this work.

The WCA technique first consists in employing a MESFET simulator in the "reverse direction" in order to extract the material and structural parameters corresponding to a nominal device from the foundry's data book. Then the MESFET simulator is used to forecast the change arising from to a process deviation.

The requirements for such a simulator are the following:

1) It should be valid for any kind of MESFET independently of the technology of fabrication, i.e., epitaxial or ion-implanted active layer, planar or recessed structure.
2) The input data should be basic geometrical or electrical information readily available to circuit designers.
3) It should provide an equivalent circuit for any bias condition, including the "cold" FET case ($V_{DS} = 0$ V) in order to use it with a network analysis program.
4) It should allow a good physical understanding of device behavior. Then the model will also work as a troubleshooting tool.
5) It has to be practical, easy to handle, and fast to run as required for circuit design. Our goal was to execute the model on a personal computer.

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TABLE I
PROCESS VARIATIONS AFFECTING MMIC ELEMENT PERFORMANCE

	Fabrication step	Affected parameter	Concerned element
1	S.I. substrate, Interface with active zone	μ_o , K_{SUB}	MESFET GaAs resistors
2	Doping of active zone, activation of donors	N_D, X_{ED}	MESFET GaAs resistors
3	Ohmic contact realization	R_S, R_D	MESFET, GaAs resistors
4	Etching of gate recess	A	MESFET
5	Gate lithography	L	MESFET
6	Thin Film Deposition	C_S (pF/mm^2) $R_\square$ (ohm)	MIM capacitors Metallic resistors
7	Surface Passivation	X_{ED}	MESFET
8	Substrate thinning	H	Transmission lines Spiral inductors

K_{SUB} and X_{ED} are explained in Section II.

6) The accuracy of the results needs to be at least better than what can be guaranteed on actual devices by the manufacturer.

In fact there is little interest in developing a model whose accuracy is far better than the reproducibility (from wafer to wafer) and the uniformity (all over the wafer) of the manufacturer's technology [4]. The MESFET simulator presented here fits these demands well.

II. DESCRIPTION OF THE MESFET SIMULATOR

A. Preliminaries

The modeling of MESFET's benefits from many years of extensive effort in fabrication, measurement, and theory, upon which the work presented here is based [5]–[13]. To fulfill the requirements presented above it is clear that the model should be analytical or semianalytical, hence a straightforward resolution of a set of analytical equations.

The main input data are the geometrical dimensions (gate length and width, electrode spacing) and also the saturation current I_{DSS} (taken at $V_{GS} = 0$ V) and the gate pinch-off voltage V_p. From these quantities, which are easily available or measurable, an equivalent uniform doping (N_D, A) is first extracted. It must be noted that A represents the thickness of the active layer beneath the gate; therefore it implicitly includes the recess depth (if the case applies).

It is well known that the shape of the actual doping profile has a certain influence on the MESFET parameters [14]. For instance, it has been shown that the performance of a MMIC amplifier is affected by the energy and the dose of the active layer ion implantation [15]. In fact, the two approaches are not really contradictory because different implanted profiles, with the same pinch-off voltage, also present different values of equivalent N_D and A.

Nevertheless in some specific applications, such as buried-layer MESFET's for improved linearity, our model is certainly not valid. However this does not concern the transistors available from most MMIC foundries. Also, a knowledge of the exact doping profile $N_D(Y)$ and the exact recess depth is generally not available to the MMIC designer.

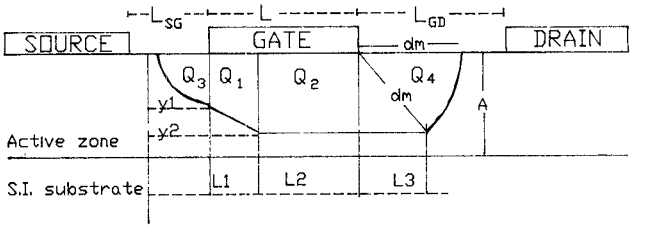

Fig. 1. Cross section of GaAs MESFET operating in saturation.

B. Basic Parameters

After setting an initial value for N_D, the electron mobility is obtained, depending on the doping value, according to [15]

$$\mu_0 = \frac{\mu}{1+\sqrt{N_D}} \tag{1}$$

where N_D is expressed in $(10^{17} \times \mathrm{cm}^{-3})$. The parameter μ has been fixed at 6000 cm^2 V^{-1} s^{-1} for all the simulations.

A two-piece velocity–electric field characteristic is used [9]:

$$v(E) = \mu_0 E/(1+E/E_0) \qquad \text{if } E \leqslant E_S \tag{2a}$$

$$v(E) = v_s \qquad \text{if } E > E_S \tag{2b}$$

where E_S is the GaAs saturation electric field and E_0 is a parameter giving the continuity of eqs. (2).

The influence of velocity overshoot in submicrometer-gate MESFET's is taken into account using the approximate formula proposed in [16]:

$$v_s(\mathrm{m/s}) = 60 \times L^{-0.56} \tag{3}$$

where L is the gate length expressed in m. Next, the active layer effective thickness under the gate is calculated depending on the pinch-off voltage as follows:

$$A = \sqrt{\frac{2\epsilon}{qN_D}(V_{\mathrm{bi}} - V_p)} \tag{4}$$

where ϵ is the GaAs permittivity and V_{bi} the Schottky built-in barrier. The saturation current for $V_{DS} = 3$ V and $V_{GS} = 0$ V is computed (see Appendix I) and is compared to the value of saturation current I_{DSS} given as input data. If they are equal the program continues; otherwise the initial value of N_D is changed and the calculations begin from (1) again.

C. Drain–Source Current and Depletion Charge Bias Model

The drain–source current I_{DS} and the total charge Q_T of the depleted zone are the two fundamental quantities on which the calculations of many of the RF parameters are based.

The cross section of the device is displayed on Fig. 1, indicating the geometry of the depleted region and the associated variables.

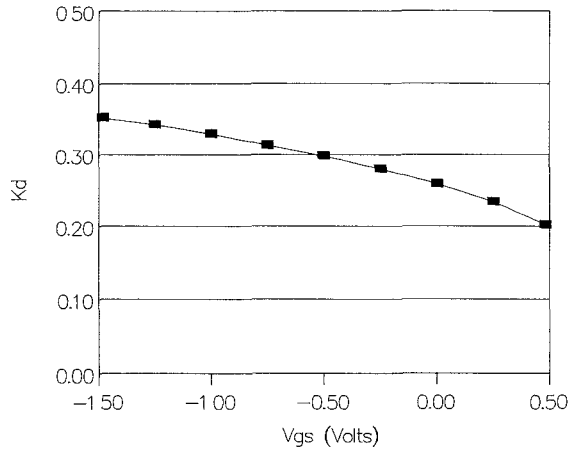

Fig. 2. Variation of the domain parameter K_d with gate-source voltage ($V_{DS} = 3$ V, $L = 0.5$ μm).

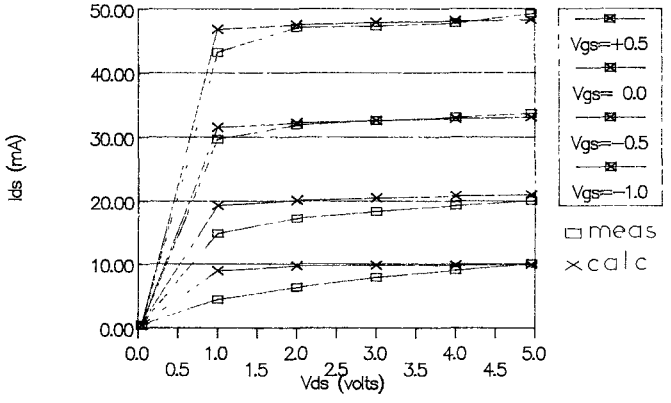

Fig. 3. Comparison of theoretical and experimental I_{DS} characteristics for a 0.5 μm × 200 μm gate MESFET.

The depleted depths y_1 and y_2, the length L_1 of the linear part of the channel (where $v(E) < v_s$), the length L_2 of the saturated part (where $v(E) = v_s$), and the length L_3 of the extension of the saturated region towards the drain are computed as well as I_{DS} for any couple of dc voltages (V_{GS}, V_{DS}). The calculations are detailed in Appendix I.

The respective voltage drops across these parts of the channel, V_1, V_2, and V_3, are also obtained. The originality of this model has to do with the calculation of the domain parameter defined in [12] and [17] and is equal to

$$K_d = \frac{V_2}{V_2 + V_3}. \tag{5}$$

K_d is not empirical and constant, but varies smoothly with V_{GS}, as suggested in [17] (Fig. 2).

A comparison between calculated and measured values of I_{DS} for a 0.5-μm-gate-length MESFET is given in Fig. 3. This device belongs to the MMIC technology presented in Section IV. Even though it has an implanted doping profile, the agreement with the simulation is satisfactory. The observed differences are discussed in subsection III-B.

The total charge Q_T is the sum of the charges corresponding to the different regions under the gate, Q_1 ($0 < x < L_1$) and Q_2 ($L_1 < x < L_2$), with the extensions of the depleted zone towards the source Q_3 and towards the drain Q_4. The extension towards the source is assumed to be a quarter arc with a radius equal to y_1, and the area towards the drain is considered as half a rectangle ($L_3 \times y_2$) plus an arc of radius d_M [9] (see Fig. 1). However, the reality of these "edge" effects can be different because:

i) Those geometric assumptions are somewhat approximative.
ii) The surface doping density might differ from the constant N_D used in the calculations.
iii) The presence of a surface potential which depletes a thin region between the MESFET electrodes. This potential is difficult to evaluate and may depend on the quality of the dielectric passivation.

For these three reasons, Q_3 and Q_4 are multiplied by an empirical "edge" factor X_{ED} as shown in the following relation:

$$Q_T = Q_1 + Q_2 + X_{ED}(Q_3 + Q_4). \tag{6}$$

A typical X_{ED} value for half-micron-gate MESFET's from different manufacturers is between 0.8 and 1.8.

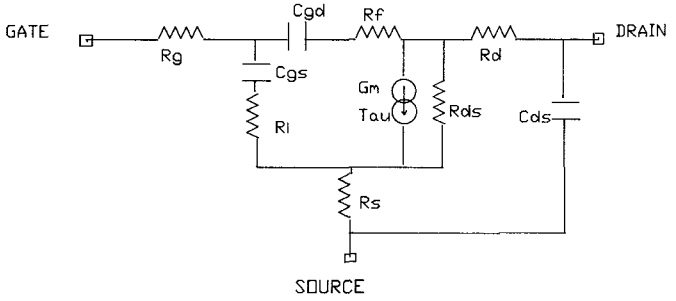

Fig. 4 MESFET equivalent circuit.

D. Elements of the MESFET Equivalent Circuit

The simulator calculates an equivalent circuit with nine elements among the 11 of Fig. 4.

The extrinsic transconductance G_{me} is obtained by incrementing V_{GS} and calculating the change in I_{DS}. Then the intrinsic transconductance G_m is derived with the method described in Appendix II. There is no fitting parameter for G_m calculation.

It is well known that it is very difficult to determine exactly the RF value of the output resistance R_{ds}, which is lower than the dc value. The reason comes probably from effects of the substrate–active layer interface, which vary from one manufacturer to an other. Thus, a parallel resistance R_{SUB} is added to the intrinsic dc output resistance, and R_{ds} becomes

$$R_{ds} = \left| R_{ds\,dc}^{-1} + R_{SUB}^{-1} \right|^{-1}. \tag{7}$$

R_{SUB} accounts for a RF contribution of the saturated part of the channel with a length equal to $L_2 + L_3$ and is given by

$$R_{SUB} = K_{SUB}(L_2 + L_3)/Z \tag{8}$$

where Z is the total width of the device and K_{SUB} is a

parameter having the dimension of a resistance per square. K_{SUB} is held to fit the nominal value of R_{ds} of the investigated device at a given bias condition. Then K_{SUB} is assumed to be a material constant and does not vary with doping, active layer thickness, gate length, or applied voltage. However since L_2 and L_3 change with those conditions (Appendix I), R_{SUB} and finally R_{ds} will also change.

The variations of Q_T in response to the variations of applied voltages V_{GS}, V_{DS} give the extrinsic values of C_{GS} and C_{GD}. The intrinsic values are extracted as discussed in Appendix II. One obtains

$$C_{gs} = \left| \frac{\Delta Q_T}{\Delta V_{gs}} \right|_{V_{dg} = \text{constant}} \tag{9}$$

and

$$C_{gd} = \left| \frac{\Delta Q_T}{\Delta V_{dg}} \right|_{V_{gs} = \text{constant}} \tag{10}$$

With these definitions it can be verified that for a perfectly symmetric device ($L_{SG} = L_{GD}$), C_{gs} and C_{gd} become equal when $V_{DS} = 0$ V (cold FET). The parameter X_{ED}, included in Q_T, is also assumed to be a material constant. It is adjusted to fit the C_{gs} of a nominal device at a given bias condition. Then only the four charge values (Q_1 to Q_4) are bias dependent and give a satisfactory capacitance–voltage characteristic for the device. The same X_{ED} is used for C_{gs} and C_{gd} calculations. Finally a contribution of fringing capacitances, totally bias-independent, is included in the simulator (Appendix III).

Considering that the depletion capacitance C_{gs} is in fact distributed beneath the gate with a channel resistance, it is possible to compute the input resistance R_i of Fig. 4 [9], [15].

The same method applied to C_{gd} allows the determination of the feedback resistance R_F. The value of R_F is negligible when V_{DS} is above the knee voltage (i.e., $V_{DS} > 2$ V) but is comparable to R_i when V_{DS} is very small. Therefore the equivalent circuit of Fig. 4 is symmetric and valid for "cold" FET operation as required for many switch, attenuator, and phase-shifter designs.

The experimental value of C_{DS} is generally found to be bias independent. Then it should be considered as a parasitic element of the MESFET and is calculated as the capacitance originating from the electrostatic coupling of source and drain metallization lines [6]. It depends mainly on the source–drain distance L_{SD} and also on the contact size (See Appendix III).

The transit time associated with the transconductance is assumed to be dependent on the length of the saturated region only. Then Tau is read as

$$\text{Tau} = \frac{(L_2 + L_3)}{v_s} \tag{11}$$

The gate resistance is independent of applied voltages and is given by [18]:

$$R_G = \frac{R_{\square G} Z}{3N^2 L} \tag{12}$$

where N is the number of gate fingers, Z the total width, and $R_{\square G}$ the resistance per square of the gate metallization. These data are usually always available to the designer.

The access resistances R_S and R_D are not calculated by the simulator because they are too dependent on the technology of fabrication (i.e., planar or recessed structure). Unless a close relationship exists between the manufacturer and the designer of the circuit, it is not possible to forecast their values. Therefore the R_S and R_D values of a nominal device are entered in the program as input data. The access resistance is the sum of a term due to ohmic contact resistivity plus the resistance of the semiconductor between the ohmic contact and the depletion region. This last term is dependent on technological parameters such as doping concentration, recess depth, and gate–source (or drain) distance. Then any variation of those parameters will change the nominal value of the access resistance.

E. Noise Parameters of the MESFET

It is often useful to predict the noise parameters of the MESFET for, at least, a qualitative study. The approach used here is based upon the FET noise theory developed in [6] and [19].

The relationships between the four noise parameters and equivalent circuit elements are

$$F_{\min} = 1 + 2(\omega C_{gs}/G_m) P_1 + 2(\omega C_{gs}/G_m)^2 P_2 \tag{13a}$$

with

$$P_1 = \sqrt{Kg(Kr + G_m(R_S + R_G))} \tag{13b}$$

$$P_2 = KgG_m(R_S + R_G + KcR_i) \tag{13c}$$

where

$$\omega = 2 \times \pi \times f \quad (f \text{ in Hz})$$

$$Rop = \sqrt{G_m(R_S + R_G) + Kr} \Big/ \left(\sqrt{Kg} \times C_{gs}\omega\right) \tag{14}$$

$$Xop = Kc/(C_{gs}\omega) \tag{15}$$

$$Rn = \left(Kc^2 Kg + G_m(R_S + R_G) + Kr\right) / \left(G_m \times (1 + Kx^2\omega^2)\right) \tag{16}$$

Details of the derivation of factors Kg, Kr, and Kc are given in [6]. The new parameter Kx has been introduced to take into account the decrease of noise resistance Rn when frequency increases. This behavior is always ascertained experimentally for GaAs MESFET's [20] and could not be predicted with the original theory, which leads to a frequency-independent expression for Rn.

The values of the four factors have been set to 2.53, 0.01, 0.81, and 5.3 10^{-12} for Kg, Kr, Kc, and Kx, respectively, to fit the actual data of one particular manufacturer for the MESFET and at the operating condition described in Section IV. Therefore these factors may change from one technology to another.

TABLE II
ERROR FUNCTION COEFFICIENT AND DIFFERENCES BETWEEN THEORETICAL AND EXPERIMENTAL S PARAMETERS (AT 15 GHz) FOR FIVE DIFFERENT GaAs MANUFACTURERS

FOUNDRY	A	B	C	D	E
ϵ (%)	1.95	2.45	2.33	4.41	7.58
MAG(S_{11}) dB	0.4	0.1	0.05	0.75	0.75
MAG(S_{22}) dB	0.4	0.4	0.3	0.1	0.5
MAG(S_{21}) dB	0.3	0.1	0.1	0.4	0.55
ANG(S_{21}) deg	4	7	5.7	8.2	1.5

III. VERIFICATION AND LIMITATIONS OF THE MESFET SIMULATOR

A. Comparison Between Simulation and Measurement

S parameters of MESFET's from five different GaAs foundries have been fitted to extract the experimental values of the equivalent circuit detailed in Fig. 4. In every case, the bias conditions are $V_{DS} = 3$ V and $I_{DSS}/2$, and the dimensions of the gate are $L = 0.5$ μm and $Z = 300$ μm. Using the nominal data provided by the manufacturer (L_{SD}, number of gate fingers, $I_{DSS}, V_p, R_S, R_D, R_{\square G}$), a theoretical equivalent circuit has been computed by the simulator for each device. Only device C is epitaxial, i.e., having a uniform doping; the others are ion implanted.

Table II shows a comparison of error function coefficients calculated by the circuit analysis software TOUCHSTONE [21] when starting a "MODEL optimization." It can roughly be described as the average divergence of the square of theoretical S parameters from the square of experimental S parameters. The averaging is done over the frequency range (1–20 GHz) with a 200 MHz step. The error function coefficient combines the results of the four S parameters.

For sake of comparison, a variation of +10 percent on C_{gs} and C_{gd} together with −10 percent on G_m and R_{ds}, made on the experimental device E, gives $\epsilon = 9$ percent. For device E, which demonstrates the poorest agreement, Fig. 5(a) and (b) shows the difference in the amplitude and in the phase of the theoretical and experimental S parameters. Over the four S parameters the disparities never exceed 7° in phase, 1 dB in amplitude of S_{11} or S_{22}, and 1.5 dB in amplitude of S_{21}.

To go deeper in detail, Table II also gives the differences found at 15 GHz between theory and experiment for the magnitudes of S_{11}, S_{22}, and S_{21} and the phase of S_{21}. Even at such a frequency these numbers are still very small for all of the five devices investigated.

Because the simulations are very satisfactory, the MESFET model may now permit the investigation of the influence of deviations in the process of fabrication. To illustrate the breadth of these deviations, we have displayed in Table III the range of variation for I_{DSS} and V_P tolerated on the PCM (process control monitor) by the five foundries.

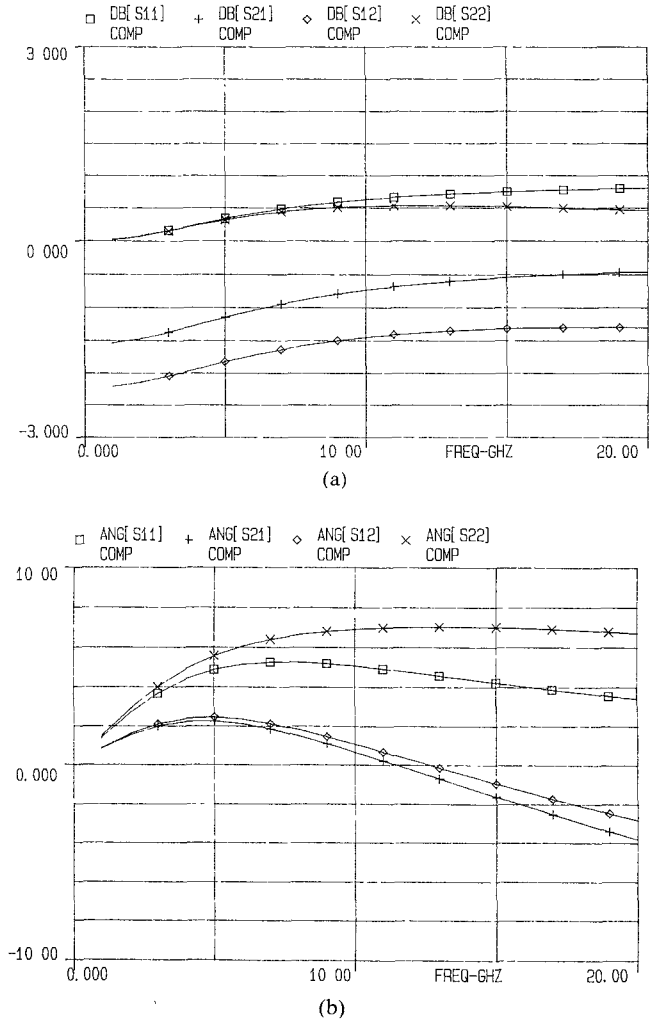

Fig. 5. Disparity between experimental and theoretical S parameters of a 0.5 μm×300 μm gate MESFET from foundry E (a) Difference of amplitudes. (b) Difference of phases. Operating conditions. $V_{DS} = 3$ V, $I_{DSS}/2$.

B. Limitations of the Simulator

When presenting a model it is always advisable to describe its limits.

- The phenomena intervening at large drain bias [22], such as electron temperature effect, the presence of a high electric field at the drain side of the depleted region, or strong injection of carriers into the substrate, have not been included in the simulator. Therefore the simulator is not recommended for operating with V_{DS} greater than 5 V, as with power FET simulations.
- Because of the uniform doping approximation, the model might not be valid for certain ion-implanted devices operating near pinch-off where the channel doping differs too much from the average value. This

TABLE III
MAXIMAL ALLOWED ELECTRICAL DEVIATIONS FOR FIVE GaAs FOUNDRIES

FOUNDRY	A	B	C	D	E
$I_{DSS}(\%)^{\pm}$	33	47	25	40	28
$Vp^{\pm}$ (%)	20	48	36	35	19

occurs approximately when I_{DS} is lower than 10 percent of I_{DSS}.

- The model does not account for a dc current leakage through the substrate. Actually this seems to be the case for some real devices and affects the characteristics of the MESFET in two ways:
  a) It shifts the value of V_P when V_{DS} increases, and gives resistive $I_{DS}(V_{DS})$ characteristics when V_{GS} approaches the pinch-off. For these reasons also our model is not fully valid when I_{DS} is lower than 10 percent of I_{DSS}.
  b) It changes the value of the dc R_{ds} term in (7). Therefore the simulation of R_{ds} is correct when simulating around specific bias conditions but is not perfectly suitable to describe R_{ds} versus V_{DS} or V_{GS} characteristics. (In fact according to this model, R_{ds} should increase when V_{GS} is more negative and it is indeed the case for foundries D and E. However for foundries B and C, R_{ds} decreases and it starts decreasing and then increases for foundry A.)

  An implementation is perhaps to add a dc leakage current in the substrate I_{SUB} as in [23]. This implementation is the object of investigation.

IV. APPLICATION TO THE DESIGN OF A LOW-NOISE MMIC AMPLIFIER

A. Process-Dependent WCA

The goal was to design a 15 dB gain cascadable module having a relatively broad band around 4 GHz with low-noise performance. The specifications are summarized as follows:

Bandwidth:	3.5–4.5 GHz.
Gain:	15 dB.
Gain flatness:	1 dB_{pp}.
Return losses:	< -15 dB.
Noise figure:	< 3.5 dB.

The circuit was fabricated by the THOMSON-DAG GaAs foundry using a double ion implantation for the formation of the active layer. The gate metal is deposited onto the active layer after a recessing of the top highly doped region. E-beam lithography is used for gate length definition (0.5 μm). The manufacturer allows I_{DSS} to vary from 9 to 21 mA and V_p from -0.7 to -1.3 V [24]. The MESFET simulator indicates that this corresponds to a combination of ± 10, 6, and 6 percent arbitrary deviations on L, N_D, and A, respectively.

Combining those dispersions a best case and a worst case (in terms of gain) can be determined. Then an equivalent circuit is computed for each situation and the elements are reported on Table IV for a 0.5 μm MESFET with two fingers of 75 μm.

It must be emphasized that all parameters are computed values only. A process sensitivity can now be performed on the MMIC using the S parameters and noise parameters corresponding to each case of Table IV.

The amplifier is a two-stage configuration. The chip includes LC matching and dc biasing networks. The chip size is 1.5 mm $\times$ 2.5 mm. A photograph of the fabricated circuit is shown in Fig. 6.

The simulated results obtained using TOUCHSTONE [21] are displayed for the nominal and the two extreme cases for the gain, noise figure, and input and output return losses in Fig. 7(a), (b), (c), and (d) respectively. The worst case in terms of gain corresponds also to poor noise performance. Return losses are not significantly affected by the MESFET parameter since they depend mainly on the matching networks.

It can be seen that, as far as the gain and the return losses are concerned, even the worst cases meet the specifications. This was made possible by the following method:

i) Tighten the specifications for the nominal case design.
ii) Adopt a very conservative design always using the foundry's standard elements, which are well characterized.

Ranges of possible variation of each element of the MESFET ($G_m, C_{gs}, R_{ds}, C_{gd}$, etc.) are given in the foundry's data book. Using these data in our circuit analysis software [21], a WCA has been achieved.

The results, also displayed on Fig. 7, are pessimistic and probably not realistic because they correspond to an unlucky combination of interdependent parameters taken without correlation. This demonstrates the superiority of the process-dependent WCA.

B. Experimental MMIC Results

Fig. 7 also shows for comparison typical results obtained from realized circuits. They are well inside the predicted window for gain and noise performance. The input and the output matching of the amplifier are excellent. Two wafers were processed. Of 66 chips, 43 were good after dc testing (65 percent yield) and among them 28 passed the RF testing, leading to a 42 percent overall yield.

Fig. 8 presents a histogram of the distribution of the small-signal gain (dB $|S_{21}|$) taken at the lowest useful frequency (3.5 GHz) where the gain is the smallest. Most of the measured gains are between 15 and 16 dB.

Fig. 9 shows the measured values of the noise figure at the extreme and center frequencies for six devices. The result is satisfactory.

TABLE IV
COMPUTED VARIATIONS OF MESFET PARAMETERS FOR NOMINAL, BEST, AND WORST CASES

	I_{DSS} mA	V_P V	$R_S + R_D$ ohms	G_m mS	Tau ps	R_{ds} ohms	C_{gs} fF	R_i ohms	C_{gd} fF	C_{DS} fF	R_G ohms	F_{min} dB
Nominal case	15	-1	5.4	15.6	4	381	103	14.3	23.1	36.5	1.7	0.51
Best case	21	-1.3	4.2	17.2	3.6	322	100.5	4.6	23	36.5	1.9	0.45
Worst case	9.7	-0.7	6.6	14.4	4.3	391	106.5	29.5	22.5	36.5	1.6	0.58

Equivalent circuit elements are calculated at $V_{DS} = 3$ V, $I_{DSS}/2$; F_{min} at 4 GHz.

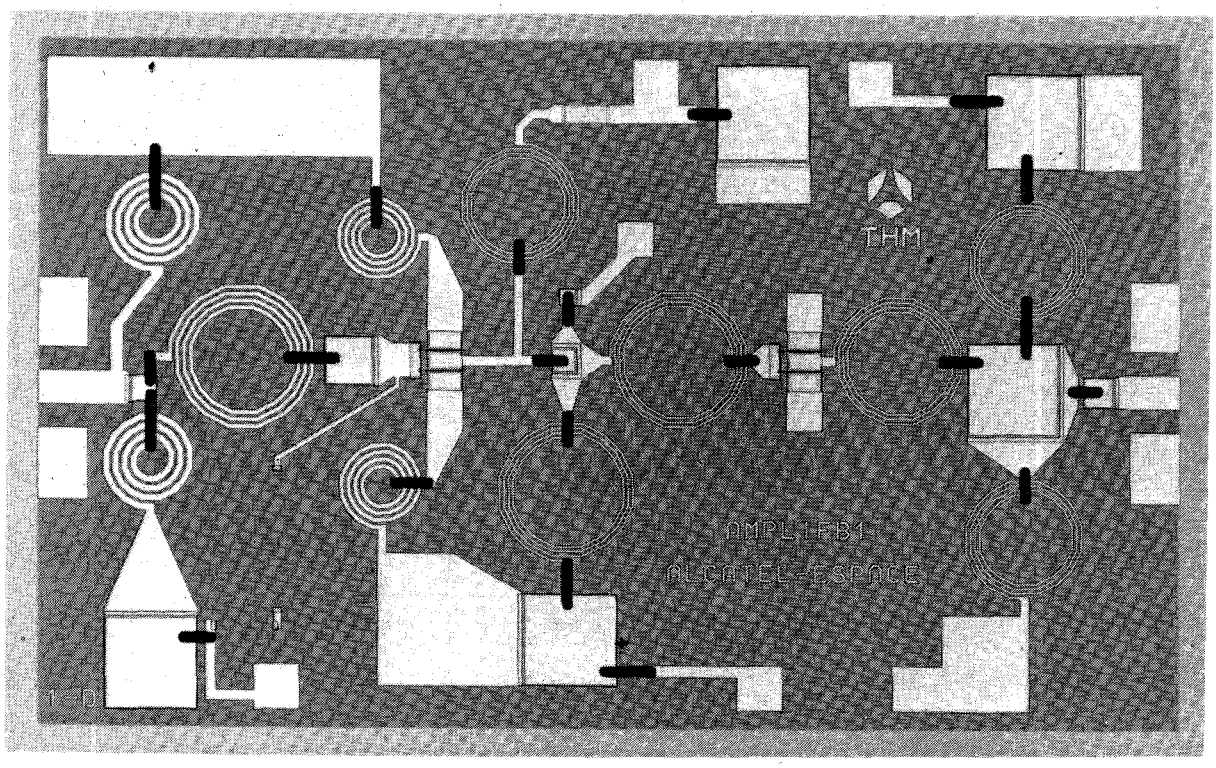

Fig. 6. Fabricated MMIC C-band amplifier. Chip size: 1.5×2.5 mm^2.

V. CONCLUSION

Cost reduction is the major concern of designers willing to insert MMIC's in large projects such as phased array antennas. Therefore a worst-case analysis of the envisaged circuit becomes as important as the electrical design itself. A reliable WCA has to be carried out using process-dependent parameter dispersions rather than uncorrelated electrical deviations, which implies the use of physical models of the MMIC elements.

The simulator presented here for the MESFET is very convenient, easy to handle, and fast to run as required for circuit analysis. The calculations of static characteristics, elements of the equivalent circuit, and noise parameters have been detailed. The simulator has also been verified by recomputing the data from five different GaAs foundries.

Obviously, this MESFET model is a tool which can find other applications. For example, it can predict the influence of aging of dc supplies on circuit performance. It has been successfully used for a MMIC amplifier design. The high value of the overall RF yield (42 percent) is evidence of the process quality, and also accounts for the conservative method adopted in designing practice.

APPENDIX I
I_{DS} CALCULATION

A subroutine in the program computes I_{DS} given the dc bias (V_{DS}, V_{GS}). The saturated regime corresponds to a V_{DS} large enough to obtain either:

$$d_M \geq A \qquad (d_M \text{ defined below})$$

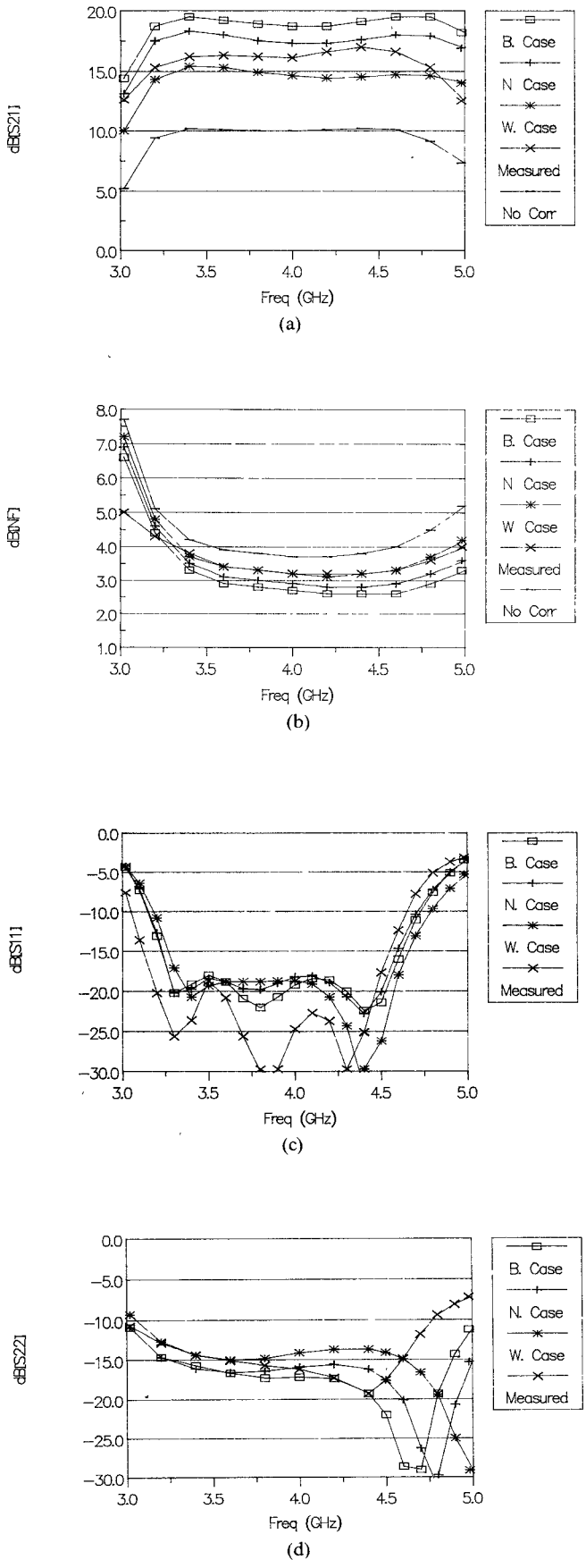

Fig. 7. Comparison of simulated (nominal, best, and worst cases) and measured MMIC amplifier performance. "No Corr" represents the WCA from elements without correlation. (a) Gain. (b) Noise figure. (c) Input return loss. (d) Output return loss.

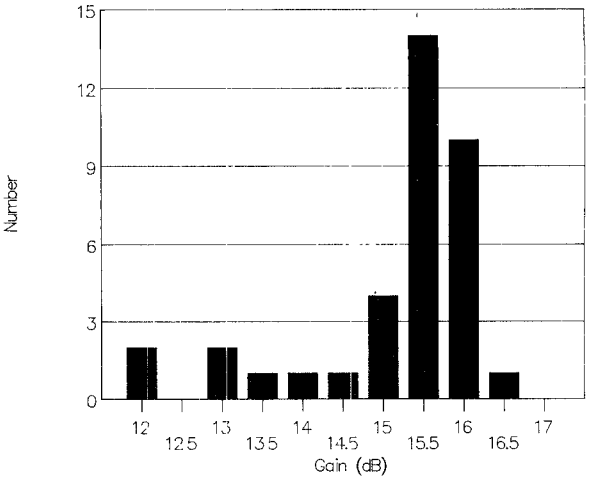

Fig. 8. Histogram of gain distribution from 36 amplifiers measured at 3.5 GHz. Chips come from two wafers.

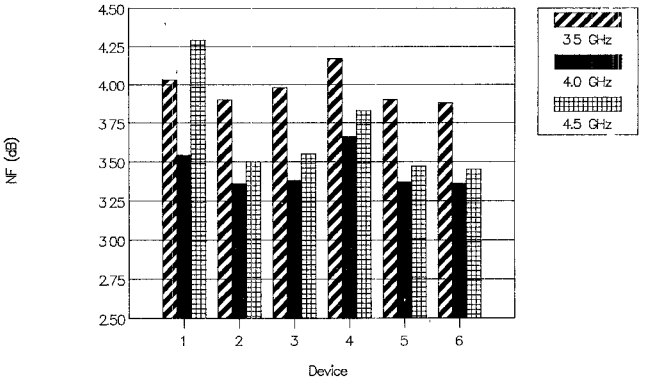

Fig 9. Measured values of the amplifier noise figure at 3.5, 4, and 4.5 GHz. Six circuits were measured ($V_{DS} = 3$ V, $I_{DSS}/2$).

or

$$I_{DS} \geq qv_s ZN_D(A - d_M).$$

In this case, I_{DS} should satisfy the following set of equations.

Depleted depths (see Fig. 1):

$$y_1 = \sqrt{\frac{2\epsilon}{qN_D}(V_{bi} - V_{GS} + R_S I_{DS})} \tag{A1}$$

$$y_2 = A - I_{DS}/(qv_s ZN_D). \tag{A2}$$

Depth of maximal extension towards the drain:

$$d_M = \sqrt{\frac{2\epsilon}{qN_D}(V_{DS} - V_{bi} - V_{GS} - R_D I_{DS})}. \tag{A3}$$

Channel extension towards the drain:

$$L_3^2 = d_M^2 - y_2^2. \tag{A4}$$

Voltage drop in regions 1, 2, and 3:

$$V_1 = \frac{qN_D}{2\epsilon}\left(y_2^2 - y_1^2\right) \tag{A5}$$

$$V_2 = \frac{2y_2}{\pi} E_S \sinh\left(\frac{\pi L_2}{2y_2}\right) \quad [5], [9], [23] \tag{A6}$$

$$V_3 = L_3 E_S \cosh\left(\frac{\pi L_2}{2y_2}\right) \quad [25]. \tag{A7}$$

Current in the linear region:

$$I_{DS}\left(L_1 + \frac{V_1}{E_0}\right) = \frac{q^2 Z \mu_0 N_D^2}{\epsilon}\left|A\frac{\left(y_2^2 - y_1^2\right)}{2} - \frac{\left(y_2^3 - y_1^3\right)}{3}\right|. \tag{A8}$$

For the linear regime (low V_{DS}) only (A1), (A3), (A5), and (A8) apply with $L = L_1$, $y_2 = d_M$, and $V_2 = V_3 = 0$.

Appendix II
Relationships Between Extrinsic and Intrinsic Parameters

1) The relationships between extrinsic (V_{DS}, V_{GS}) and intrinsic (V_{ds}, V_{gs}) voltages are

$$V_{DS} = v_{ds} + (R_S + R_D) I_{DS}$$
$$V_{GS} = v_{gs} + R_S I_{DS}$$
$$V_{DG} = v_{dg} + R_D I_{DS}.$$

2) By differentiating I_{DS} with respect to extrinsic and intrinsic voltages and identifying the different terms, one obtains [26]

$$G_m = \left|\frac{\Delta I_{DS}}{\Delta v_{gs}}\right|_{v_{ds}} = \frac{G_{me}}{1 - R_S G_{me} - (R_S + R_D) G_{de}}$$

and

$$G_d = \left|\frac{\Delta I_{DS}}{\Delta v_{ds}}\right|_{v_{gs}} = \frac{G_{de}}{1 - R_S G_{me} - (R_S + R_D) G_{de}}$$

where

$$G_{me} = \left|\frac{\Delta I_{DS}}{\Delta V_{GS}}\right|_{V_{DS}} \quad \text{and} \quad G_{de} = \left|\frac{\Delta I_{DS}}{\Delta V_{DS}}\right|_{V_{GS}}$$

are the extrinsic values.

3) With a comparable operation concerning the total depletion charge Q_T one finds

$$C_{gs} = \left|\frac{\Delta Q_T}{\Delta v_{gs}}\right|_{v_{dg}} = C_{GS} + (G_m + G_d)(C_{GS} R_S + C_{GD} R_D)$$

and

$$C_{gd} = \left|\frac{\Delta Q_T}{\Delta v_{dg}}\right|_{v_{gs}} = C_{GD} + G_d (C_{GS} R_S + C_{GD} R_D)$$

where

$$C_{GS} = \left|\frac{\Delta Q_T}{\Delta V_{GS}}\right|_{V_{DG}} \quad \text{and} \quad C_{GD} = \left|\frac{\Delta Q_T}{\Delta V_{DG}}\right|_{V_{GS}}$$

are the extrinsic values.

Appendix III
Calculation of Fringing Capacitances

The fringing capacitance is equal to [6]

$$C_F = (\epsilon_0 + \epsilon) C_R Z$$

where Z is the total width of the device, and ϵ_0 and ϵ are the absolute permittivity of air and GaAs respectively. The parameter C_R is computed as follows:

$$C_R = \frac{1}{\pi} \ln\left|2\left(1 + \sqrt{C_{KP}}\right)\Big/\left(1 - \sqrt{C_{KP}}\right)\right| \quad \text{if } C_K < 1/\sqrt{2}$$

$$C_R = \frac{1}{\pi} \ln\left|2\left(1 + \sqrt{C_K}\right)\Big/\left(1 - \sqrt{C_K}\right)\right|^{-1} \quad \text{if } K \geq 1/\sqrt{2}$$

with

$$C_{KP} = \sqrt{1 - C_K^2}.$$

The factor C_K is different for the C_{DS} case and for the C_{GS} and C_{GD} cases [6].

C_{DS} case:

$$C_K = \sqrt{(2W_0 + L_{SD}) L_{SD} / (W_0 + L_{SD})^2}$$

where W_0 represents the width of the MESFET ohmic contact.

C_{GS} and C_{GD} case:

$$C_K = \sqrt{L_{SG} / (L + L_{SG})}.$$

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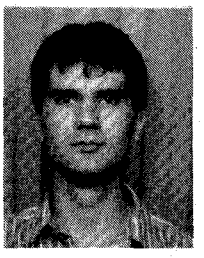

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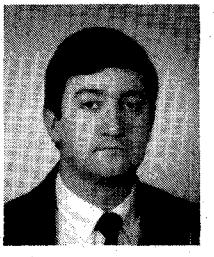

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